

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng, et al. Docket No.: TSM03-0698
Serial No.: 10/786,643 Art Unit: TBD
Filed: February 25, 2004 Examiner: TBD
For: CMOS Structure and Related Method


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Date of Deposit: March 11, 2004

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Information Disclosure Statement (1 page)
IDS Form PTO/SB/08a and 08b (2 pages) citing (10) references
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Respectfully submitted,


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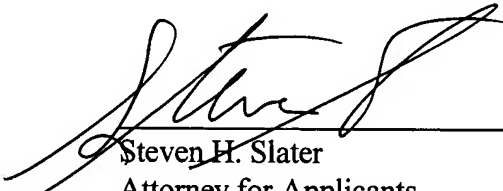
Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a & 08b that may be considered material to the examination of the above-identified application.

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Respectfully submitted,

March 11, 2004

Date


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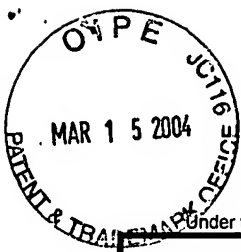


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STATEMENT BY APPLICANT**

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2

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Complete if Known

Application Number 10786,643

Filing Date February 25, 2004

First Named Inventor Cheng, et al.

Art Unit TBD

Examiner Name TBD

Attorney Docket Number TSM03-0698

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	2	Rim, K., et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1406-1415, July 2000.	
	3	Rim, K., "Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology," IEEE International Solid-State Circuits Conference, paper #7.3, pp. 116-117, 2001.	
	4	Yeo, Y.C., et al., "Enhanced performance in Sub-100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium," International Electron Device Meetings, pp. 753-756, 2000.	
	5	Ootsuka, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meetings, pp. 575-578, 2000.	
	6	Ito, S., et al., "Mechanical Stress Effect of Etch-Stop Nitride and Its Impact on Deep Submicron Transistor Design," International Electron Device Meetings, pp. 247-250, 2000.	
	7	Shimizu, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," International Electron Device Meetings, pp. 433-436, 2001.	
	8	Ota, K., et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," International Electron Device Meetings, pp. 27-30, 2002.	
	9	Scott, G., et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," International Electron Device Meetings, pp. 827-830, 1999.	
	10	Bianchi, R.A., et al., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," International Electron Device Meetings, pp. 117-120, 2002.	

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